IN THE CLAIMS

40. (previously presented) Integrated circuitry comprising:

a semiconductive substrate;

an electrically insulating layer over the semiconductive substrate; and

a series of alternating first and second conductive lines spaced and positioned laterally adjacent one another over the insulating layer, the first lines and the second lines having respective line tops, and being electrically isolated from one another laterally by intervening insulating spacers having respective spacer tops that are substantially coplanar with at least some of the first and second line tops.

41. (previously presented) The integrated circuitry of claim 40 wherein at least some of the individual laterally adjacent first and second series lines are disposed directly on the electrically insulating layer.

42. (previously presented) The integrated circuitry of claim 40 wherein the first lines have a substantially common lateral cross sectional shape and the second lines have a substantially common lateral cross sectional shape, the first lines' lateral cross sectional shape being different from the second lines' lateral cross sectional shape.

43. (previously presented) The integrated circuitry of claim 40 wherein the first and second conductive lines constitute the same materials.

44. (previously presented) The integrated circuitry of claim 40 wherein the first and second conductive lines constitute different materials.

45. (previously presented) The integrated circuitry of claim 40 wherein the first conductive lines predominately comprise undoped polysilicon and the second conductive lines predominately comprise metal.

46. (previously presented) The integrated circuitry of claim 40 wherein the first conductive lines predominately comprise doped polysilicon and the second conductive lines predominately comprise metal.

47. (previously presented) The integrated circuitry of claim 40 comprising a plurality of the series of the first and second conductive lines at multiple elevations relative to the substrate.

48. (previously presented) Integrated circuitry comprising:

a semiconductive substrate;

a layer of electrically insulating material over the semiconductive substrate; and

a series of alternating first and second conductive lines over the layer of insulating material, the first and second lines having respective lateral widths and being spaced and positioned laterally adjacent one another, the first lines and the second lines being electrically isolated and separated from one another laterally by intervening strips of insulating material having respective individual insulating material lateral widths that are substantially less than the lateral widths of any of the first and second conductive lines, none of the first and second lines overlapping any immediately laterally adjacent first or second lines.

49. (previously presented) The integrated circuitry of claim 48 wherein each of the first and second lines are disposed on and in contact with the layer of insulating material.

50. (previously presented) The integrated circuitry of claim 48 wherein the first lines have a substantially common lateral cross sectional shape and the second lines have a substantially common lateral cross sectional shape, the first lines' lateral cross sectional shape being different from the second lines' lateral cross sectional shape.

51. (previously presented) The integrated circuitry of claim 48 wherein the first and second conductive lines constitute the same materials.

52. (previously presented) The integrated circuitry of claim 48 wherein the first and second conductive lines constitute different materials.

53. (previously presented) The integrated circuitry of claim 48 wherein the first conductive lines predominately comprise undoped polysilicon and the second conductive lines predominately comprise metal.

54. (previously presented) The integrated circuitry of claim 48 wherein the first conductive lines predominately comprise doped polysilicon and the second conductive lines predominately comprise metal.

55. (previously presented) The integrated circuitry of claim 48 comprising a plurality of the series of the first and second conductive lines at multiple elevations relative to the substrate.

56. (previously presented) Integrated circuitry comprising:

a semiconductive substrate;

an electrically insulative borophosphosilicate glass (BPSG) layer over the semiconductive substrate;

a series of first conductive polysilicon lines over the BPSG layer, the first series conductive lines having individual pairs of respective sidewalls;

electrically insulative oxide material over respective first series conductive lines, a top of the oxide material over at least some of the lines defining a first plane;

a plurality of insulative oxide sidewall spacer pairs, individual spacer pairs being on respective sidewall pairs of individual first series conductive lines and being connected with the electrically insulating oxide material over the respective individual first series conductive lines;

individual first series conductive lines being effectively insulated by the BPSG layer, the respective sidewall spacer pairs, and the respective insulating oxide material; and

a series of second conductive aluminum-containing lines having respective line tops at least some of which define a second plane that is coplanar with said first plane, the series of second conductive lines being over the BPSG layer.

57. (previously presented) The integrated circuitry of claim 56, wherein first series conductive lines have elevational thicknesses in a range from 2000 Angstroms to 10,000 Angstroms.

58. (previously presented) The integrated circuitry of claim 56, wherein individual second series lines have substantially a common lateral cross sectional shape.

59. (new) A semiconductor processing method of forming a plurality of conductive lines comprising:

forming an electrically insulating layer over a semiconductive substrate;

forming a series of alternating first and second conductive lines spaced and positioned laterally adjacent one another over the insulating layer, the first lines and the second lines having respective line tops; and

forming intervening insulating spacers having respective spacer tops that are substantially coplanar with at least some of the first and second line tops, the first lines and the second lines being electrically isolated from one another laterally by the intervening insulating spacers.

60. (new) The method of claim 59 wherein the first lines have a substantially common lateral cross sectional shape and the second lines have a substantially common lateral cross sectional shape, the first lines' lateral cross sectional shape being different from the second lines' lateral cross sectional shape.

61. (new) The method of claim 59 wherein the first and second conductive lines constitute different materials.

62. (new) The method of claim 59 comprising a plurality of the series of the first and second conductive lines at multiple elevations relative to the substrate.

63. (new) A semiconductor processing method of forming a plurality of conductive lines comprising:

forming a layer of electrically insulating material over a semiconductive substrate;

forming a series of alternating first and second conductive lines over the layer of insulating material, the first and second lines having respective lateral widths and being spaced and positioned laterally adjacent one another; and

forming intervening strips of insulating material having respective individual insulating material lateral widths that are substantially less than the lateral widths of any of the first and second conductive lines, the first lines and the second lines being electrically isolated and separated from one another laterally by the intervening strips of insulating material, none of the first and second lines overlapping any immediately laterally adjacent first or second lines.

64. (new) The method of claim 63 wherein the first lines have a substantially common lateral cross sectional shape and the second lines have a substantially common lateral cross sectional shape, the first lines' lateral cross sectional shape being different from the second lines' lateral cross sectional shape.

65. (new) The method of claim 63 wherein the first and second conductive lines constitute different materials.

66. (new) The method of claim 63 comprising a plurality of the series of the first and second conductive lines at multiple elevations relative to the substrate.

67. (new) A semiconductor processing method of forming a plurality of conductive lines comprising:

forming an electrically insulative borophosphosilicate glass (BPSG) layer over a semiconductive substrate;

forming a series of first conductive polysilicon lines over the BPSG layer, the first series conductive lines having individual pairs of respective sidewalls;

forming electrically insulative oxide material over respective first series conductive lines, a top of the oxide material over at least some of the lines defining a first plane;

forming a plurality of insulative oxide sidewall spacer pairs, individual spacer pairs being on respective sidewall pairs of individual first series conductive lines and being connected with the electrically insulating oxide material over the respective individual first series conductive lines;

effectively insulating individual first series conductive lines with the BPSG layer, the respective sidewall spacer pairs, and the respective insulating oxide material; and

forming a series of second conductive aluminum-containing lines having respective line tops at least some of which define a second plane that is coplanar with said first plane, the series of second conductive lines being over the BPSG layer.

68. (new) The integrated circuitry of claim 67, wherein first series conductive lines have elevational thicknesses in a range from 2000 Angstroms to 10,000 Angstroms.

69. (new) The integrated circuitry of claim 67, wherein individual second series lines have substantially a common lateral cross sectional shape.